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LOW VOLTAGE AND HIGH FIELD-EFFECT MOBILITY THIN FILM TRANSISTOR USING CRYSTALLINE POLYMER NANOCOMPOSITE AS GATE DIELECTRIC

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Abstract: Anthracene thin-film transistor (TFT) with an ultrathin layer (~450nm) of Poly-vinylidene fluoride (PVDF)/CuO nanocomposites as a gate insulator have been fabricated. A device with excellent electrical characteristics at low operating voltages has been designed. Different layers of the film were also prepared to achieve the best optimization of ideal gate insulator with various static dielectric constant (εr). Capacitance density, leakage current at 1V gate voltage and electrical characteristics of OFETs with a single and multi layer films were investigated. This device was found to have highest field effect mobility of 2.27 cm2/Vs, a threshold voltage of 0.34V, an exceptionally low sub threshold slope of 380 mV/decade and an on/off ratio of 106. The output characteristic of OFET after poling were changed and exhibited linear current-voltage relationship showing the evidence of large polarization. The stable performance of the OFET after poling operation makes it reliable in temperature sensor applications. Such High-ε CuO/PVDF gate dielectric appears to be highly promising candidates for organic non-volatile memory and sensor field-effect transistors (FETs).

Keywords: Organic Field Effect Transistors, gate dielectric, thin film transistor, Organic semiconductor

INTRODUCTION

Organic Field Effect Transistors (OFETs) are drawing much more attention during the last few years due to their reasonably lower cost, higher performance and good compatibility with flexible electronic applications such as memory, radio frequency identification, sensors etc. [1-5] Despite a number of interesting properties the traditional materials (silicon, silicon dioxide etc.) have reached their fundamental material limits in the device performance in scaled devices due to its very low dielectric constant(k=3.9) where gate material with high dielectric constant is necessary to enable the required drive currents for sub-micrometer devices. Further if we decrease the thickness of SiO_2 (~ 2nm) the leakage current dominates. These high leakage currents will invariably compromise the device performance as well as dissipate large amount of power. Again typically, $d/L \leq 0.1$ is necessary to ensure that the field created by gate to source voltage (V_G) and not the lateral field, drain to source voltage(V_D), determines the charge distribution within the channel. This technology introduces inexpensive, low temperature processability and large area device processing as well as enables new device functions. To fully realize the flexibility aspects in OFET technology, it is essential to develop polymer based gate dielectrics that may be fabricated via easy solution processing.

Polymers as gate dielectrics have smooth surfaces and afford appropriate surface tension to improve the crystallinity and molecular ordering of the organic semiconductor layer grown on gate dielectric surface. Low voltage operation is possible by reducing the threshold voltage and subthreshold slope (*SS*), SS (=$dV_{GS}/d(\log I_{DS})$) which are mainly controlled by the properties of gate dielectric rather than organic semiconductors. So, for low operating voltage a high capacitance is required to induce a high density of free carriers at the channel. The field induced current is proportional to the free carrier density induced at the channel-dielectric interface and mobility (μ) of

the organic semiconductor. Hence, to overcome high operating voltage requirement either high capacitance gate dielectric can be used or, thickness of the gate dielectric layer should be reduced. Several research groups have fabricated OFETs by using polymers and polymer composites. Organic semiconductors have been widely studied from the view point of their fundamental optoelectronic properties and their potential applications such as organic light emitting diode (OLED), organic field effect transistors (OFETs), photovoltaic cells etc. In the case of acene group of organic semiconductors, pentacene exhibits the highest mobility (μ=3.0cm^2/Vs) among OFETs. However, chemical modification of pentacene has a difficulty due to its low solubility in common organic solvents as well as instability in air. Hence, anthracene has attracted our attention because of its better solubility. The OFETs with anthracene as organic semiconductor exhibits efficient charge transportation systems.

In this paper, a low voltage operable OFET with high-k PVDF-CuO nanocomposite gate dielectric layer and benzanthracene as organic semiconductor have been fabricated for temperature sensing applications. A very simple fabrication process has been used along with step wise poling process for enhancing the pyroelctric effects on the device performance. The output characteristic of OFET after poling were changed and exhibited linear current-voltage relationship showing the evidence of large polarization. The temperature dependent response of the device was also investigated. The stable performance of the OFET after poling operation makes it reliable in temperature sensor applications.

EXPERIMENTAL SECTION

CuO nanoparticles were prepared by the sol-gel method by reacting at room temperature acquous solutions of copper nitrate and sodium hydroxide at pH=10. The resulting gel was washed several times with distilled water until free of nitrate ions. This gel was then centrifuged and dried in air. The PVDF powder was purchased from Aldrich(99.9%) and N,N-Dimethyleformamide (DMF) from Merch(99.5%). A desired amount of CuO nanoparticles were completely dispersed in 80mL DMF in an ultrasonic bath for 10hours. The calculated quantity of PVDF (such that the amount of CuO in the composite is 10wt% of PVDF) were added into the above suspension and stirred well for 7hours to dissolve the PVDF completely. ITO(Indium Tin Oxide) coated glass was used as substrate where ITO layer was used as gate electrode(G). Now for the formation of the gate dielectric layer cleaned ITO coated glass was dipped into the solution of PVDF-CuO composite in an angle 35º for 15minutes. Then it was lift-off the solution slowly. The sample was dried at 60ºC for 2hours to remove DMF completely. Next, the sample with gate dielectric layer was annealed on a hot plate at 150ºC so that the PVDF-CuO composite layer melted completely and then it was maintained at this temperature for 3 hours. After that it was cooled naturally upto room temperature in nitrogen atmosphere. We used Anthracene (Aldrich, 98%pure) as organic semiconductor and toluene (Merck, 99.5% pure) as solvent. Required amount of Anthracene powder was added with toluene and stirred in a water bath for 72 hours. The solution was then remained still for atleast 5hours. Subsequently, the organic semiconductor layer was deposited on gate dielectric layer by dip coating process and dried at room temperature. Source(S) and drain(D) electrodes were deposited by a gold coater unit. The thickness of the anthracene thin film was measured by an atomic force microscope (AFM, Park System, XE 100) and was found to be 74 nm using the tapping mode. The transistor characteristics of the anthracene-OTFT were measured by using a KEITHLEY Model 4200-SCS semiconductor characterization system in a dark box at room temperature. Au source/drain top electrodes onto this film were deposited by a thermal evaporation method using a tungsten basket. These electrodes with 100 nm thickness were made through the shadow mask.

RESULTS AND DISCUSSION

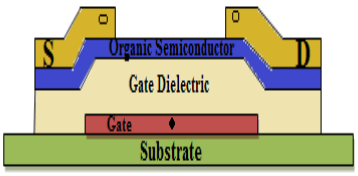

Fig. 1. Schematic diagram of the as-prepared anthracene Organic thin-film transistor structure with PVDF/CuO nanocomposite as gate dielectric.

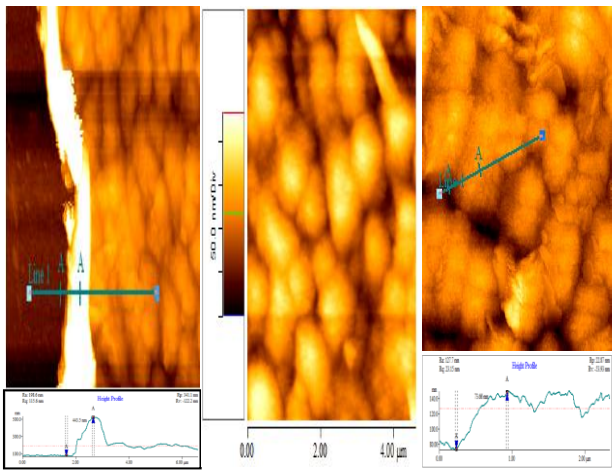

Fig. 2.(a) The AFM image and height profile for a cross-linked PVDF film blended with 10 vol% CuO nanoparticles. (b) One-dimensional AFM images of anthracene film. (c) Thickness of the anthracene TFT using PVDF/CuO composite as gate dielectric as revealed from AFM image.

The schematic structure of the benzanthracene-OTFT is shown in Fig. 1 of the on chip poling process where the source (S) and drain (D) electrodes were grounded and gate electrode was connected to a negative bias. The organic semiconductor layer (Benzanthracene in this case) and gate electrode (ITO in this case) acted as poling electrode and a uniform poling electric field was produced across the gate dielectric (PVDF/CuO composite) layer. The surface morphology of the benzanthracene thin film was examined using an AFM. The AFM images in three dimensional of the organic active layer are shown in Fig. 2a and b. As seen in Fig. 2a and b, the benzanthracene thin film is formed from homogeneous small crystal grains with an average diameter about 200 nm. The roughness for the benzanthracene thin film was found to be 3.878 nm. The roughness and grain size parameters are important parameters affecting electrical performance of OTFTs. As displayed in the AFM image (Fig. 2b), PVDF polymer layer showed a pinhole-free and very smooth surface with root mean square (RMS) roughness of 0.144 nm within a 5×5 mm2 scan scale. The smooth dielectric surface is essential for the well-ordered anthracene molecular stacking. Charge transport takes place primarily within the first few layers of semiconductor molecules near the semiconductor/insulator interface and the device performance is dominated by these interfacial layers. AFM image of a 2 nm thick anthracene layer was captured to examine the surface morphology, as given in Fig. 2c. The image shows that the initial layer of molecules fully covered the substrate in a flat 2D plane except for a few small voids. The rms roughness of the dielectric film with 10 vol% GO nanoparticles is ~12.8 nm, which is much rougher than that of the pure crossed-linked PVDF film (~0.3 nm). This suggests that there are probably some defects present in the gate insulator, which may cause the current leakage. This problem is likely to be resolved in the future by engineering the nanoparticle with side groups soluble in organic solvent. The morphology of the polymer thin film will be smoothened, subsequently reducing the leakage current.

The output characteristics (drain current, I_D vs. drain-source voltage, V_{DS}) at different gate-source voltage, V_G of the Organic Field Effect Transistor (OFET) before poling shown in Fig. 3(a) are similar to those of conventional ferroelectric field effect transistors (FeFETs).[26-27] As seen in Fig. 3, the drain current increases with drain voltage and reaches a saturation due to a pinch-off of the active channel of the transistor. The benzanthracene OFET works in a p-channel operational mode because the drain current increases with negative gate voltages. This indicates that benzanthracene has p-type charge transport material. One of the interesting features of these devices is the saturation of drain current (I_D) at higher drain-source voltage (V_{DS}). Contrastingly, for the present device, the saturation occurs, for example, at a drain-source voltage (V_{DS}) of ~ -0.5V for a gate-source voltage (V_{GS}) of -0.2V. It is clearly seen that the operating voltage is much lower compared to those of similar other reported works.[28] One of the reason behind this might be for the use of PVDF/CuO composite as gate dielectric whose capacitance is sufficiently large (C_i=32.18nF). The operating voltage of OFET depends critically on the nature of gate dielectric materials and their interfacial properties, because the surface of the gate dielectric material make a contact with the channel through which drain current flows. Hence, a gate dielectric of higher capacitance induces higher charge injection into the organic semiconductor layer at a particular gate voltage, allowing a lower operating voltage. Figure 3(b) shows the transfer characteristic of the device from where we calculated the transconductance,[29] of about 17µS at V_{DS}= -0.5V close to the highest reported so far for SWCNT-FETs [30] and testifies superior gate coupling and to a large carrier field-effect mobility. The device exhibits a threshold voltage between -0.05 and -0.5 V, depending on whether the threshold voltage is estimated from the plot of the square root of the drain current versus gate-source voltage or from the plot of the drain current versus drain-source voltage. PVDF/CuO is a p-type semiconductor and the device operates in the accumulation mode. However, since the turn-off voltage is small compared to practical supply voltages, the full ON/OFF ratio between accumulation and depletion can be exploited in many circuit applications. It is typically 10^6 (between Vg=0.1 V and Vg=+0.5 V) but on some samples ON/OFF ratios as high as 10^7 have been obtained. The turn-on characteristics are sharp with a small subthreshold slope S= $[d(\log Isd)/dVg]^{-1}$ of 0.4 V/decade. To the best of our knowledge, these are the best ON/OFF characteristics reported for an organic TFT. They are comparable to that of an a-Si TFT.[31]

Charge carrier mobilities, however, are still an order of magnitude lower than for a-Si. From the transfer characteristics in the saturation regime, the mobility is extracted according to the following relation[31]

$$I_{SD} = \frac{W \times C_i}{2 \times L} \cdot \mu_{FE}^{sat} \cdot (V_G - V_T)^2 \quad (1)$$

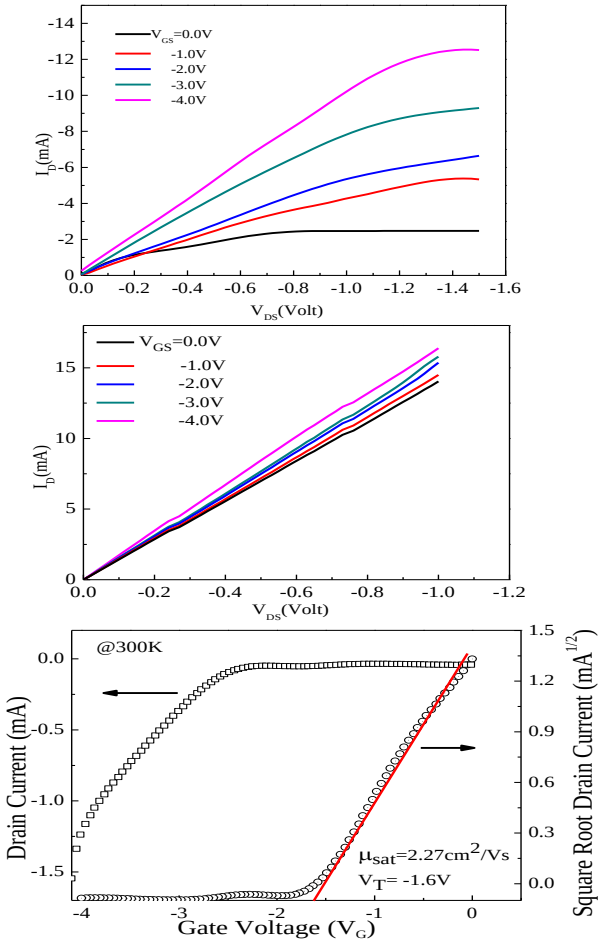

Fig. 3 (a) I_D vs. drain-source voltage, V_{DS} at different V_G(b) shows the transfer characteristic (c) I_D and Sq. root of I_D as a function of V_G

Where μ is the field-effect mobility, C_i=32.18 nF/cm^2 is insulator (PVDF/CuO dielectric layer) capacitance, and W and L are the width and length of the channel, respectively, and V_T is the threshold voltage. The average field-effect mobility was a 1.1±0.1 cm^2/V-s (measured at a gate-source voltage of −1 V, i.e., the drain saturation voltage), a threshold voltage of 0.34 V, a subthreshold slope of 0.38V/decade and an on/off current ratio of 10^6 were obtained. This field-effect mobility is comparable with the best mobilities reported for pentacene TFTs.[30] The subthreshold slope determines the voltage swing required for transistor to turn from "off" to "on" and should be as low as possible. Only the values for silicon-on-insulator transistors have approached the theoretical limit thus far, which is close to 60 mV/decade at room temperature.[31] A high subthreshold slope is a traditional weakness of organic transistors that results from their low gate-dielectric capacitance, which reduces swing speed. The fabrication of an OTFT with a subthreshold slope within a factor of 6 of the theoretical limit is a significant leap forward.31 This may be related to the ionic species in the polymer (PVDF in present case) dielectric film remaining from the dichromate cross-linking agent. The experimental characteristics are quadratic only in the range 0.05 V< $|V_g|$ <0.25 V and exhibit poor current saturation at higher gate voltages. Within the quadratic range we obtain values of μFE = 0.02–0.05 cm2/V s under optimized deposition conditions. The threshold voltage is low, $|V_T|$ < 0.05 V. The TFT characteristics in Fig. 1(a) reveal some non-ideal features. Near V_{DS}=0, the output characteristics is nonlinear, especially for higher gate voltages. Above V_G=-0.2 V, current saturation becomes poor and VSD has to significantly exceed $|V_G-V_T|$ to drive the transistor into saturation. These non-idealities may at least partly be related to a non-ohmic source/drain contact. Although anthracene based OFETs exhibited high device performances at low voltages, critical drawbacks, such as ID hysteresis during gate swing, were found in the transfer curve of the device. The hysteresis present during device operation led to a shift in V_{th} when the device was switched from off to on, and back to off. This phenomenon prevents this OFET from being used as a driving unit device in display backplanes or logic circuitry in radio frequency identification (RFID) tags, in which Vth must be stable. In our device, hysteresis showed a specific clockwise loop directionality: on-to-off swept transfer curves shifted towards a higher V_G compared with off-to-on sweeps.

CONCLUSION

In conclusion, we have demonstrated the potential of using ultrathin layers of PVDF/CuO as insulator for organic semiconductors by preparing a high performance device with low voltage operation. We have also shown that pyroelectric PVDF based insulators can be used to obtain organic transistors with good electrical properties with a cheap and easy process, and that the performance of such devices is significantly improved by using an ultrathin gate insulator of PVDF and their temperature sensitive behavior. The use of of a built-in pyroelectric gate dielectric would reduce the complexity of the fabrication process. The device we fabricated was found to have a field effect mobility of 1.5 cm^2/Vs (close to the best mobilities reported of pentacene TFTs), and an on/off current ratio of 10^6. Integrating various smart organic dielectric materials directly into the OFET device structure would enable the production of a vast range of functional or smart organic electronic devices.

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